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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/408,366	09/29/1999	KEISUKE HASHIMOTO	018775-765	3976

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EXAMINER	
DASTOURI, MEHRDAD	
ART UNIT	**PAPER NUMBER**
2623	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/408,366	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Mehrdad Dastouri	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicants' amendment filed August 12, 2003, has been entered and made of record.
2. Applicants' arguments have been fully considered but they are not persuasive.

Applicants indicate that the density level determining circuit of Claim 1 uses both the density level of the target pixel as well as the edge direction of the target pixel when determining the multi-level density level in the plurality of sub-pixels in the target pixel. In this respect, Applicants argue that Koizumi et al (Secondary prior art of record) do not appear to take into account the edge direction of the target pixel which includes the sub-pixels. The Examiner disagrees and indicates that Sekine et al (Primary prior art of record) disclose an image processor comprising an edge judgment circuit which discriminates an edge direction of a target pixel from the density level of the target pixel and adjacent pixels thereof based upon the multi-level image data (Figure 1,Edge Detection 13; Column 10, Lines 3-24); and a density level determining circuit which determines density levels in a plurality of sub-pixels in the target pixel, where the target pixel is divided into the sub-pixels, in accordance with the density level of the target pixel and the edge direction of the target pixel discriminated by the edge judgment circuit (Column 5, Lines 53-67, Column 6, Lines 1-2; Figures 15 and 32; Column 21, Lines 65-67, Column 22, Lines 1-37, Fifth Embodiment. As depicted in Figure 32, resolution conversion (Step 1261) is performed on the sub-pixels of the target pixel as described in Column 9, Lines 45-65 and edge information obtained by outline

developing section 124. As depicted in Figure 15, each sub-pixel has a bi-level density value of 0 or 1). Accordingly, Sekine et al alone disclose all limitations of Claim 1 by considering the dictionary definition of prefix "multi" as "two or more", that means a "bi-level" density value is a "multi-level" density value.

The teachings of Koizumi et al are merely cited for generalization of density values to more than two levels. Consequently, there is no requirement that secondary prior art (Koizumi et al) discloses the same teachings of primary prior art (Sekine et al) for concerning the edge direction of the target pixel.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 5-7, 10, 11, 15, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (U.S. 5,862,257) in view of Koizumi et al (U.S. 5,486,927).

Regarding Claim 1, Sekine et al discloses an image processor which processes multi-level image data on density levels of pixels, comprising:

an edge judgment circuit which discriminates an edge direction of a target pixel from the density level of the target pixel and adjacent pixels thereof based upon the multi-level image data (Figure 1,Edge Detection 13; Column 10, Lines 3-24); and

a density level determining circuit which determines density levels in a plurality of sub-pixels in the target pixel, where the target pixel is divided into the sub-pixels, in accordance with the density level of the target pixel and the edge direction of the target pixel discriminated by the edge judgment circuit (Column 5, Lines 53-67, Column 6, Lines 1-2; Figures 15 and 32; Column 21, Lines 65-67, Column 22, Lines 1-37, Fifth Embodiment. As depicted in Figure 32, resolution conversion (Step 1261) is performed on the sub-pixels of the target pixel as described in Column 9, Lines 45-65 and edge information obtained by outline developing section 124. As depicted in Figure 15, each sub-pixel has a bi-level density value of 0 or 1).

Sekine et al do not explicitly disclose determining multi-level density level in a plurality of sub-pixels in the target pixel.

Koizumi et al disclose a digital image forming apparatus using subdivided pixels comprising a density level determining circuit which determines multi-level density levels in a plurality of sub-pixels in the target pixel (Figures 1(a), 1(b), 2(a), 2(b), 13(a), 13(b), 14(a), 14(b), 15(a) and 15(b); Column 6, Lines 50-67, Column 7, Lines 1-16; Column 10, Lines 66-67, Column 11, Lines 1-60).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Sekine et al invention according to the teachings of Koizumi et al to determine multi-level density levels in a plurality of sub-pixels in the target pixel because it will minimize jaggedness in the image boundaries and will enhance sharpness of the image.

Regarding Claim 2, Sekine et al further disclose the image processor according to Claim 1, wherein the density level determining circuit comprises:

a density controller circuit which sets density-level setting parameters for each of the sub-pixels in the target pixel in accordance with the edge direction of the target pixel discriminated by said edge judgment circuit (Figures 5C-5D, 50C-50D and 15-17; Column 9, Lines 42-53; Column 16, Lines 63-67, Column 17, Column 18, Lines 1-5); and

a density-level setter circuit which sets the density level of each of the plurality of sub-pixels in the target pixel based upon the density level of the target pixel by using the parameters set by said density controller circuit (Figures 5C-5D; 50C-50D and 15; Column 9, Lines 54-65).

Sekine et al teachings direct to setting density level in bi-level sub-pixels. Koizumi et al teachings direct to setting density level in multi-level sub-pixels (Figures 1(a), 1(b), 2(a), 2(b), 13(a), 13(b), 14(a), 14(b), 15(a) and 15(b); Column 6, Lines 50-67, Column 7, Lines 1-16; Column 10, Lines 66-67, Column 11, Lines 1-60).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Sekine et al invention according to the teachings of Koizumi et al to set density levels in a plurality of multi-level sub-pixels in the target pixel because it will minimize jaggedness in the image boundaries and will enhance sharpness of the image.

Regarding Claim 3, Sekine et al further disclose the image processor according to Claim 1, wherein said edge judgment circuit discriminates a first edge which

represents that an edge of a character image exists in a first direction relative to the target pixel, a second edge which represents that an edge of a character image exists in a second direction opposite to the first direction relative to the target pixel, and a narrow edge which represents that a character image exists at a center of the target pixel (Figures 4 and 14; Column 16, Lines 35-49)..

Regarding Claim 5, Sekine et al further disclose the image processor according to Claim 1, further comprising:

a line width judgment circuit, which determines a width of a line including the target pixel (Figures 35-37; Column 23, Lines 20-67, Embodiment Sixth which is variation of Fifth Embodiment);

a smoothing circuit which performs smoothing on the image data of the target pixel and the adjacent pixels thereof in accordance to the line width determined by said line width judgment circuit and outputs the image data of the target pixel which have been smoothed (Figure 35, Smoothing Processing Section 1262; Column 22, Lines 10-17); wherein the density level determining circuit determines the density levels in the plurality of sub-pixels in accordance with the density level of the target pixel subjected to smoothing by said smoothing circuit and the edge direction of the target pixel discriminated by the edge judgment circuit (Resolution Conversion Section 1261; Column 21, Lines 47-62).

With regards to Claims 6 and 11, arguments analogous to those presented for Claim 2 are applicable to Claims 6 and 11.

Regarding Claim 7, Sekine et al further disclose the image processor according to Claim 6, wherein said line-width judgment circuit determines the line width of the line including the target pixel based upon the edge direction of the target pixel and those the adjacent pixels of the target pixel discriminated by the edge judgment circuit (Figures 35-37; Column 23, Lines 20-60).

Regarding Claim 10, arguments analogous to those presented for Claim 2 are applicable to Claim 10. Sekine et al further disclose utilizing filtering operation for smoothing image data but do not disclose a specific filtering process.
Silver et al disclose smoothing on image data of the pixel, on which the edge judgment circuit discriminates an edge, by using an asymmetric filter having the target pixel at a center thereof (Figures 1A-1D; Column 6, Lines 30-63).

Regarding Claim 15, arguments analogous to those presented for Claim 1 are applicable to Claim 15.

Regarding Claim 16, arguments analogous to those presented for Claim 5 are applicable to Claim 16.

With regards to Claim 18, arguments analogous to those presented for Claim 10 are applicable to Claim 18.

Regarding Claim 19, arguments analogous to those presented for Claims 1 and 2 are applicable to Claim 19.

5. Claims 4, 8, 9, 12-14, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (U.S. 5,862,257) in view of Koizumi et al (U.S. 5,486,927) and Silver et al (U.S. 6,408,109).

Regarding Claim 4, neither Sekine et al nor Koizumi et al explicitly disclose the image processor according to Claim 1, wherein said edge judgment circuit cancels the discriminated edge direction when the density level of a pixel adjacent to the target pixel in the edge direction is larger than a threshold value.

Silver et al disclose an apparatus for detecting and sub-pixel location of edges in digital images comprising an edge-direction detecting circuit that cancels the discriminated edge direction when the density level of a pixel adjacent to the target pixel in the edge direction is larger than a threshold value (Figures 4A-C, 5 and 6; Column 13, Lines 54-67, Column 14, Column 15, Lines 1-30; Tables 3-5).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Sekine et al and Koizumi et al combination according to the teachings of Silver to cancel the discriminated edge direction when the density level of a pixel adjacent to the target pixel in the edge direction is larger than a threshold value because it will enhance the extracted edge direction and improve the quality of the printed characters.

Regarding Claim 8, neither Sekine et al nor Koizumi et al explicitly disclose the image processor according to Claim 1, further comprising an edge judgment correction circuit connected to said edge judgment circuit and corrects the edge direction when the edge direction discriminated by said edge judgment circuit is not appropriate.

Silver et al disclose an apparatus for detecting and sub-pixel location of edges in digital images comprising an edge judgment correction circuit connected to the edge

judgment circuit and corrects the edge direction when the edge direction discriminated by the edge judgment circuit is not appropriate (Column 3, Lines 19-36).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Sekine et al and Koizumi et al combination according to the teachings of Silver et al to incorporate further limitations of Claim 8 because it will enhance the extracted edge direction and improve the quality of the printed characters.

With regards to Claim 9, arguments analogous to those presented for Claim 2 are applicable to Claim 9.

Regarding Claim 12, Silver et al further disclose the image processor according to Claim 10, wherein said filter is asymmetrical with respect to a direction perpendicular to which a pixel is divided into sub-pixels (Figures 1A-1D; Column 6, Lines 30-63).

Regarding Claim 13, Silver et al further disclose the image processor according to Claim 10, wherein said smoothing circuit comprises a plurality of filters and selects one of them for smoothing (Figures 1A-1D; Column 6, Lines 30-63).

Regarding Claim 14, Silver et al further disclose the image processor according to Claim 10, wherein said smoothing circuit comprises a plurality of filters and selects one of the filters which provides a minimum density level of the target pixel after the smoothing carried by the filters (Figures 1C-1D; Column 6, Lines 51-63).

With regards to Claim 17, arguments analogous to those presented for Claim 8 are applicable to Claim 17.

Regarding Claim 20, arguments analogous to those presented for Claims 1 and 4 are applicable to Claim 20.

Conclusion

6. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Mehrdad Dastouri whose telephone number is (703) 305-2438. The examiner can normally be reached on Monday to Friday from 8:00 a.m. to 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on (703) 308-6604. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-9051 for regular communications and (703) 308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center Customer Service Office whose telephone number is (703) 306-0377.

MEHRDAD DASTOURI
PRIMARY EXAMINER

Mehrdad Dastouri
Primary Examiner
Group Art Unit 2623
December 29, 2003